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| EXAMINER | |
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| CHEN, ERIC BRICE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1765 | |

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/693,024 | WIECZOREK ET AL. | |
| | Examiner | Art Unit | |
| | Eric B. Chen | 1765 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 3 is objected to because of the following informalities: apparently, "said dielectric oxide layer" should be -- said dielectric layer --. Otherwise, the term "said dielectric oxide layer" would lack the proper antecedent basis. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. Claims 1 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the Specification lacks support for the claim limitation, "without forming a masking layer." The mere absence of a positive recitation is not basis for an exclusion. MPEP § 2173.05(i).

3. Claims 2-9 and 11-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement because they are dependent on base claims 1 and 10.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (U.S. Patent Appl. Pub. No. 2003/0080389), in view of Aronowitz (U.S. Patent No. 6,033,998).

7. As to claim 1, Hu discloses a method of forming an insulating layer, the method comprising: forming a dielectric layer (12/16/20) (paragraphs 0019, 0023, 0026) with an initial thickness on an oxidizable substrate (paragraph 0019, "a physical thickness of generally between seven and twenty-five angstroms..."), said initial thickness being less than a desired design thickness for said insulating layer (paragraph 0023, "oxidation of

layer (16) may increase the physical thickness of layer (16) by a desired amount..."); introducing nitrogen (14) into said dielectric layer (12) (paragraph 20; Figure 3) without forming a masking layer above said dielectric layer (12/16/20) (Figures 2-5); and locally increasing said initial thickness of said dielectric layer (20) (paragraph 0024).

8. Hu does not expressly disclose increasing said initial thickness according to local nitrogen concentration. However, Hu discloses local variations in nitrogen concentration in dielectric layer (20) (paragraph 0029; Figure 6). Aronowitz teaches that the formation of oxynitrides ($SiO_xN_y$) in dielectric (206) act a barrier to the oxidation process (column 6, lines 55-67) and thus a different nitrogen concentration can result in a greater increase in initial thickness following oxidation (206A/206B; Figure 2F; column 6, lines 61-67; column 7, lines 1-6). Therefore, one who is skilled in the art would expect areas of localized oxidation in dielectric (20), or increasing the initial thickness according to local nitrogen concentration.

9. As to claim 2, Hu discloses that said initial thickness is locally increased by oxidizing said substrate (paragraph 0024).

10. As to claim 3, Hu discloses that said dielectric oxide layer (12/16/20) comprises silicon dioxide (paragraphs 0017, 0019) and the initial thickness is in the range of approximately 0.5-5 nm (paragraph 0019).

11. As to claim 4, Hu discloses determining a ratio of said initial thickness (paragraph 0019, "a physical thickness of generally between seven and twenty-five angstroms...") and a maximum local increase to control a specific characteristic of said insulating layer

(paragraph 0023, "two to three angstroms may be added to the physical thickness of layer (16) through oxidation process (18)...").

12. As to claim 5, Hu discloses that said ratio is determined as a target value in advance (paragraphs 0019, 0023, 0034).

13. As to claim 6, Hu discloses that said ratio is achieved by controlling at least one of said initial thickness (paragraph 0019), a process parameter while locally increasing said initial thickness, and a process parameter while introducing said nitrogen (paragraph 0020, 0021).

14. As to claim 7, Hu discloses that said dielectric layer is formed by at least one of thermal growth, rapid thermal oxidation (paragraph 0025), chemical vapor deposition, atomic layer deposition and chemical reaction (paragraph 0020).

15. As to claim 9, Hu discloses that said nitrogen is introduced into said insulating layer by exposing said substrate to a nitrous plasma (paragraph 0033).

***Claim Rejections - 35 USC § 103***

16. Claims 8 and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu, in view of Aronowitz, in further view of Streetman, *Solid State Electronic Devices*, Prentice Hall (1990).

17. As to claim 8, Hu discloses that dielectric layer (12/16/20) is formed in the process of fabricating a thin gate dielectric for a semiconductor device (paragraph 0033). Hu does not expressly disclose patterning said insulating layer as a plurality of gate insulation layers for PMOS transistors at different locations on said substrate.

However, Streetman teaches that patterning is a widely used method to form discrete feature for the manufacturing of integrated circuits (pages 337-38). Streetman further teaches that p-channel MOS transistors (or PMOS transistors) are commonly used structures (pages 300-301) and batch processing individual wafers containing millions of transistor chips (page 332). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to pattern said insulating layer as a plurality of gate insulation layers for PMOS transistors at different locations on said substrate. One who is skilled in the art would be motivated to use conventional methods, such as patterning, to form widely used PMOS transistor structures. Moreover, one who is skilled in the art would be motivated to form a plurality of transistors by batch processing, including gate insulation layers, to reduce manufacturing costs.

18. As to claim 10, Hu discloses a method, comprising: forming a silicon dioxide layer (12/16/20) (paragraphs 0019, 0023, 0026) as a base layer for a gate dielectric (paragraph 0033) with an initial thickness (paragraph 0019, "a physical thickness of generally between seven and twenty-five angstroms...") on a first area of a silicon containing semiconductor layer provided on a substrate (13) (paragraph 0018), said initial thickness being less than a desired design thickness for said insulating layer (paragraph 0023, "oxidation of layer (16) may increase the physical thickness of layer (16) by a desired amount..."); introducing nitrogen (14) into said silicon dioxide layer (12) (paragraph 20; Figure 3) without forming a masking layer above said dielectric layer (12/16/20) (Figures 2-5); and increasing said initial thickness in said first area

(paragraph 0024) and a desired thickness of said gate dielectric (paragraphs 0023, 0024, 0033).

19. Hu does not expressly disclose increasing said first area on the basis of nitrogen contained therein. However, Hu discloses local variations in nitrogen concentration in dielectric layer (20) (paragraph 0029; Figure 6). Aronowitz teaches that the formation of oxynitrides ($SiO_xN_y$) in dielectric (206) act a barrier to the oxidation process (column 6, lines 55-67) and thus a different nitrogen concentration can result in a greater increase in initial thickness following oxidation (206A/206B; Figure 2F; column 6, lines 61-67; column 7, lines 1-6). Therefore, one who is skilled in the art would expect areas of localized oxidation in dielectric (20), or increasing said first area on the basis of nitrogen contained therein.

20. Hu does not expressly disclose forming a silicon dioxide layer and increasing initial thickness in a second area. Streetman teaches batch processing individual wafers containing millions of transistor chips (page 332). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a transistor in a second area, including forming a silicon dioxide layer and increasing initial thickness in a second area. One who is skilled in the art would be motivated to form a plurality of transistors, including gate insulation layers, to reduce manufacturing costs.

21. As to claim 11, Hu discloses that said initial thickness is locally increased by oxidizing said substrate (paragraph 0024).

22. As to claim 12, Hu discloses that oxidizing said substrate is performed after introducing nitrogen into said silicon dioxide layer (paragraph 0023, 0024).

23. As to claim 13, Hu does not expressly disclose that wherein oxidizing said substrate is performed at least partially simultaneously with introducing nitrogen into said silicon dioxide layer. However, Aronowitz discloses a method, including: forming a silicon dioxide layer (206) as a base layer for a gate dielectric with an initial thickness (column 5, lines 58-65); introducing nitrogen into said silicon dioxide layer (column 6, lines 3-5); and increasing said initial thickness on the basis of a nitrogen concentration contained therein and a desired characteristic of said gate dielectric (column 6, lines 61-67; column 7, lines 1-6). Moreover, Aronowitz teaches limiting the number of high temperature treatment steps involved in processing (column 2, lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of oxidizing said substrate at least partially simultaneously with introducing nitrogen into said silicon dioxide layer. One who is skilled in art would be motivated to limit the overall thermal budget in processing the device and to reduce the number of process steps.

24. As to claim 14, Hu discloses determining a ratio of said initial thickness (paragraph 0019) and a maximum thickness increase (paragraph 0023) in one of said first and second areas to control a specific characteristic of said gate dielectric (paragraph 0033).

25. As to claim 15, Hu discloses that said ratio is determined as a target value in advance (paragraphs 0019, 0023, 0034).

26. As to claim 16, Hu discloses that said ratio is achieved by controlling at least one of said initial thickness (paragraph 0019), a process parameter while locally increasing said initial thickness, and a process parameter while introducing said nitrogen (paragraph 0020, 0021).

27. As to claim 17, Hu discloses that said dielectric layer is formed by at least one of thermal growth, rapid thermal oxidation (paragraph 0025), chemical vapor deposition, atomic layer deposition and chemical reaction (paragraph 0020).

28. As to claim 19, Hu discloses that said nitrogen is introduced into said insulating layer by exposing said substrate to a nitrous plasma (paragraph 0033).

***Response to Arguments***

29. Applicants' arguments (Applicants' Remarks, pages 8-9), filed Sept. 27, 2005, with respect to the rejection of claims 1-12 and 14-19 under 35 U.S.C. 102(b) as being anticipated by Aronowitz have been fully considered and are persuasive. Applicants have pointed out that the currently amended claims 1 and 10 lack the claim limitation of "without forming a masking layer above said dielectric layer" or "without forming a masking layer above said silicon oxide layer". Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hu and Streetman.

30. Applicants' arguments (Applicants' Remarks, pages 8-9), filed Sept. 27, 2005, with respect to the rejection of claim 13 under 35 U.S.C. 103(a) as being unpatentable over Aronowitz have been fully considered and are persuasive, as discussed above.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hu and Streetman.

***Conclusion***

31. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
Nov. 7, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER